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ORIGINAL PAPER

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Using self-assembled monolayers for controlled electrodeposition of copper into submicrometer size surface features/decrements

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Abstract This work presents the application of alkanethiols for selectively masking the main surface of copper-seed-layer-covered silicon wafer, as used for the microprocessor production. The target of the investigation was to deposit copper only in the trenches and vias (channels of various shape) of micrometer size and not over the entire surface as in the presently used methods. The procedure developed starts with filling the trenches and vias with water, which is followed by dipping the wafers in a hexane solution containing dissolved dodekanetiol. Alkanetiol adsorbs and self-organizes on copper not protected with water and blocks the electroreduction of copper ions from the bath. The trenches and vias are free from adsorbed alkanetiols due to their very limited solubility in water. The surface-blocking process works very well and may effectively simplify the copper electrodeposition for microelectronic applications. The selective electrodeposition of copper accomplished by the proposed method significantly reduces the problems associated with the removal of excess of copper from the processed circuit elements.

Keywords Electrodeposition · Copper · Alkanetiols · Surface decrements · Trenches

Introduction

Modern electronics and microfabrication require patterning of submicrometer (down to tens of nanometers) resolution. Electroplating and electrochemical microfabrication [1] are widely known and useful techniques which can fulfill these requirements. Today, wet electrochemical methods are used not only for the fabrication of printed circuit boards but also for manufacturing complex internal metallic connections inside ultra-large scale integration circuits [2, 3]. These advanced applications are possible due to the two main, parallel developments. First is a major improvement in electroplating processes, behind which is the introduction of new plating bath formulations and a better understanding of the electrochemical processes involved in the deposition of metals on various substrates including the process of superconformal electrodeposition in copper damascene plating [4–6]. The second development is the continuing improvement in the masking of the substrate surface, which allows downscaling of the feature size to the submicron range, as in modern photolithography [7] and also by using self-assembled monolayers of organic resist [8].

In recent years, the advantages of wet electrolytic plating process over vapor deposition techniques (physical and chemical vapor deposition) have become apparent. They include the following: (a) plated copper has more desirable metallurgical properties (low stress, equiaxial grain structure, and high ductility), (b) superconformal plating provides improved filling of trenches and vias (less tendency for voids formation), (c) the tools and processes used in the plating are more easily scalable to large format substrates (300-mm wafers), (d) the processing time for the plating process is shorter, thus it provides significantly higher throughput, and (e) plating is a relatively low-cost manufacturing process as tooling, raw materials, and maintenance are less expensive.

Electrolytic plating is also used to produce the interconnect wiring in the current-generation, high-performance multichip modules [9]. Copper deposition is widely used for the fabrication of copper-on-chip metal interconnections in today's semiconductor industry. A serious disadvantage of this process is the deposition of copper over the entire surface of the processed silicon. The excess of deposited metal must be removed by chemical–mechanical polishing (CMP) after deposition so that only a small fraction of the deposited material remains in the surface

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features like trenches and/or vias. This means that most of the copper reduced in the plating process forms a sort of "unwanted deposit". For this reason, a successful selective deposition of copper into selected, depleted regions of the surface structure seems to be a considerable improvement. For such micro-scale fabrication (filling the channels), more advanced methods of masking of the primary surface before the metal electrodeposition are required. The use of self-assembled monolayers (SAM) creates new possibilities for increasing the degree of circuit integration. A good example here is the electron beam lithography work done on the passivated by a SAM surface [10]. The use of SAMs offers a chance to transfer sub-micrometric patterns [11–15] and enables the manufacturing of surface details whose sizes are comparable to molecular dimensions. The above examples concern the formation of patterns on flat surfaces. In this work, we demonstrate some aspects of effective application of alkanethiols for building selective blocking films on an unmodified surface before copper plating into such surface decrements as channels/trenches and vias.

Experimental

Electrochemical studies were done using an EG&G PAR 273 potentiostat. All potentials are referred to a Ag/AgCl reference electrode or a large-area copper rod electrode submersed in the copper plating bath solution.

All depositions were done under potentiostatic regime using the acid copper plating bath solution Techni ACR PC 65. Measurements were made on circa 1-cm^2 coupons of TaN and copper-seeded test wafers (1,000-Å-thick Cu seed layer) obtained from WaferNet (San Jose, CA, USA).

The surface structure of the wafers was monitored with a LEO model 435 VP scanning electron microscope.

All chemicals used in experiments were reagent grade; deionized water (Milipore-Q system) was used for solution preparation and rinsing.

Results

It is well known that alkanothiols form compact insulating barriers that may effectively inhibit the reduction processes occurring at various metallic surfaces including copper [16–18]. An effectively assembled film may totally block metal deposition processes, as these processes are usually quite sensitive to the surface modifications. Only at prolonged times (tens of minutes) nanoparticles of Cu may appear at decanethiol-covered Au surface [19]. The adsorption process of alkanethiols is potential dependent, so the blocking effect will change from maximum blockage (full coverage) to the unaffected metal deposition depending on the potential applied to the electrode. The effectiveness of alkanethiol (dodecanethiol in this case) to block the copper deposition process was evaluated for conditions typical for a copper acid electroplating bath. In strongly acidic solutions (almost 2 M H_2SO_4 in the high-acid version and circa 0.1 M H_2SO_4 in a low-acid copper plating baths), the desorption of dodecanethiol begins at circa −0.4 V (vs Ag/AgCl). The surface coverage by dodecanethiol decreases due to its desorption, and the inhibition of copper deposition becomes ineffective at the potentials more negative than −0.4 V. The effect of potential dependent adsorption of an alkanethiol on copper reduction is clearly illustrated by the voltammograms in Fig. 1. A comparison of the shapes of the Cu(II) reduction curves, obtained at the "clean" electrode surface (Fig. 1a) and that treated with dodecanethiol (Fig. 1b) indicates that the effective blocking of copper deposition at the electrode covered by a thiol layer takes place at the reduction potentials positive vs −0.35 V. A sudden increase in the reduction current visible in Fig. 1b at a potential more negative than −0.35 V reflects the decomposition of the blocking layer and the desorption of the thiol.

Basing on these findings, a potential range from −0.25 to −0.3 V (vs Ag/AgCl) was selected for the localized deposition of copper into the wafer surface features. In this range, copper is not deposited on the surface blocked by the thiols but fills the surface features where the copper seed layer remained uncovered.

Selective blocking of the main wafer surface

A micro-structured Cu-seeded silicon wafer with various micrometer-sized features was used as a standard substrate. Wafers were cut into small coupons with individual surface areas of about 1 cm^2. Each coupon contained features of various shapes and sizes, commonly used in microelectronics.

For blocking the main surface that should not be plated with copper, the self-assembled monolayer of mid-chain alcanethiol, dodecanothiol, was used. The layer was formed using a 3-mM solution in hexane. It was necessary to use a solvent that does not mix with water. The controlled deposition was done in the following way.

A wafer coupon was immersed in water for about 20 s. A small amount of wetting agent was added to the water phase to promote the penetration of water into the small

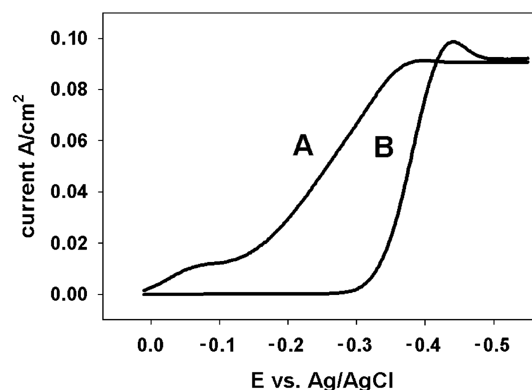

Fig. 1 Linear scan voltammograms obtained in a high-acid copper plating bath. Working electrode: copper-seeded wafer coupon of surface area ~1 cm^2. **a** Clean electrode surface. **b** Electrode blocked by dodecanethiol SAM. Scan rate 10 mV/s

surface features. Then, the coupon was taken out from the beaker and the water remaining on the flat surface of the wafer was removed carefully using a stream of inert gas (argon) directed parallel to the wafer surface. In this way, water remained in the surface features. After removal of the water from the main surface, the coupon was immersed in a solution of 3 mM dodecanethiol in hexane. It was found that a 2–3 min contact with dodecanethiol solution resulted in the formation of an optimal SAM for effective blocking of the copper deposition. After formation of a passive dodecanothiol monolayer on the wafer surface, the silicon wafer was removed from the thiol solution, dried, and cleaned by dipping it into water.

As a result of the above treatment, the passive SAM was formed only on the flat portion of the wafer that was exposed to dodecanethiol. Simultaneously, the water remaining inside small features protected the inside of the surface features from being blocked by the thiol ions. Finally, copper electrodeposition took place only inside the features. A general scheme of selective blocking of the wafer surface using mid-chain alkanethiol is shown in Fig. 2a,b.

Plating procedure

After the surface-blocking step, the coupons were removed from distilled water and placed in a copper plating bath solution. Technic ACR PC 65 acid-copper-bath formulation was used in the deposition process. Deposition was performed under potentiostatic conditions, using a three-electrode system at a potential of −0.25 to −0.3 V vs saturated Ag/AgCl electrode. The potential was applied with a short delay after the sample was placed in the bath. In the performed experiments, the time of deposition was varied from 1 to 15 min. The solution was not stirred during the plating step. The best results were obtained with plating times of 3–5 min. The results of controlled copper deposition on selectively blocked wafer are shown in Fig. 3.

Optimization of deposition process—quality of deposit

To achieve the required selective deposition, the appropriate times of SAM formation and of electrodeposition

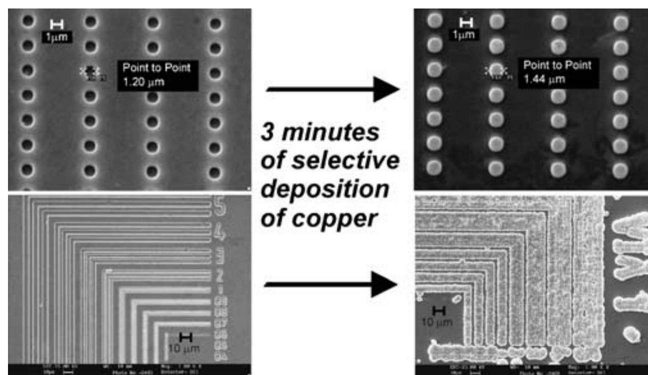

Fig. 3 Results of selective copper deposition on test wafer. Before deposition, flat surfaces were blocked by SAM of dodecanethiol

step had to be determined, as it is known that a too-short incubation time in dodecanethiol solution leads to decreased insulating properties of the SAM. An examination of the time of SAM formation and the thiol concentration indicated that the optimal time required for building a compact and effective SAM from a 3-mM solution of dodecanethiol is in the range of 120–180 s. For shorter assembly times, the monolayer is not compact enough, and copper is also partially deposited on the flat surface. The result of an experiment with too short SAM formation time is illustrated in Fig. 4. It is clear that if the time of the formation of the SAM is short, the copper can be effectively deposited inside the surface features. However, the effectiveness of an imperfectly formed SAM to block the copper deposition onto the flat surface is not sufficient, and undesirable islands of copper deposit are present at the flat surface of the coupon. A side result seen in Fig. 4 is an effect of "sliding" of the SAM layer, which is caused by incomplete coverage of the surface. On the other hand, if the coupon is in contact with the thiol solution for too long a time (longer than 300 s in 3-mM solution of dedecanethiol in hexane), the thiol has enough time to penetrate the small features. This results in a partially uncontrolled blockage of the feature walls. Consequently, the blocked portions of the features are not plated with copper, and undesired discontinuities (voids) in the copper deposit inside the features are created, making the entire approach useless.

Another point of consideration was the optimal deposition time. The important aim of the investigation was to form a deposit filling just perfectly inside of the gaps and to

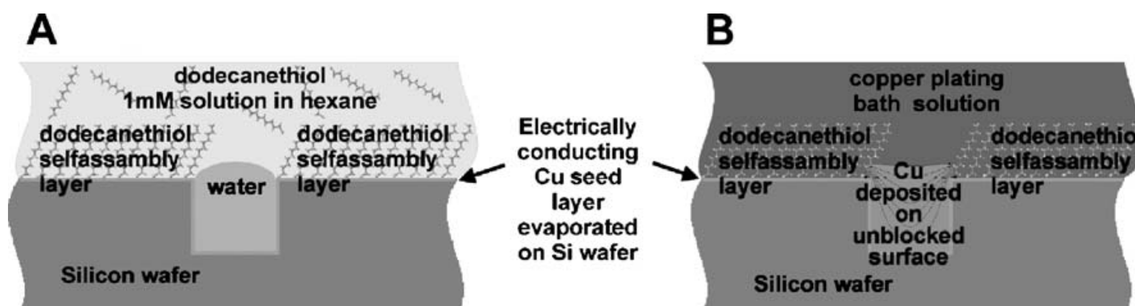

Fig. 2 Scheme for selective copper plating using alcanethiol SAM for surface blocking

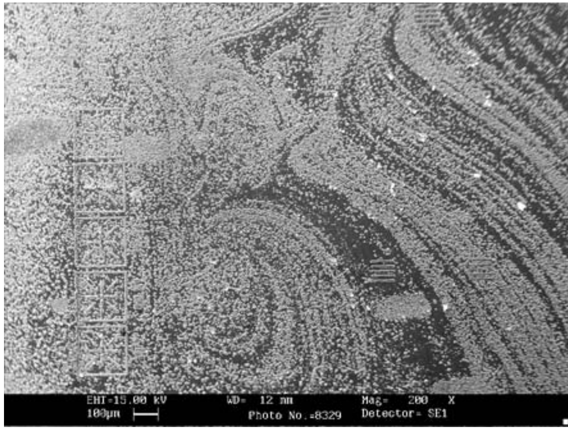

Fig. 4 Deposits on an incompletely blocked wafer

avoid developing a thick overdeposit. Obviously, this deposition time will be different for different sizes of the surface features and has to be optimized accordingly.

In our case, the result of a well-optimized copper-deposition time is shown in Fig. 5, where an optimal filling of 1-μm trenches and vias was accomplished with 150–180 s deposition time. Other conditions were the following:

- potentiostatic deposition at −0.3 V vs saturated Ag/AgCl or at −0.35 V vs Cu large-area anode immersed in the plating bath solution
- high-acid copper plating bath, Technic ACR PC 65 (ca. 0.25 M Cu in 2 M H_2SO_4)
- quiescent solution

Under the above conditions, copper completely filled the features and did not form oversized deposits. For longer plating times, the deposit grows around filled features, becomes thicker, and may form a bulky cover over the adjacent structures eventually, as it is shown in Fig. 6.

Finally, an experiment with a partially blocked surface was performed. A silicon wafer was submersed in the thiol solution only partially (~50%) leaving the remaining surface thiol-free (no dodecanethiol adsorption). The result is seen in Fig. 7, where a scanning electron microscopy image of the wafer after copper deposition is presented. The line in Fig. 7 reflects the boundary of the thiol solution during the blocking step. The Cu deposit covers the entire

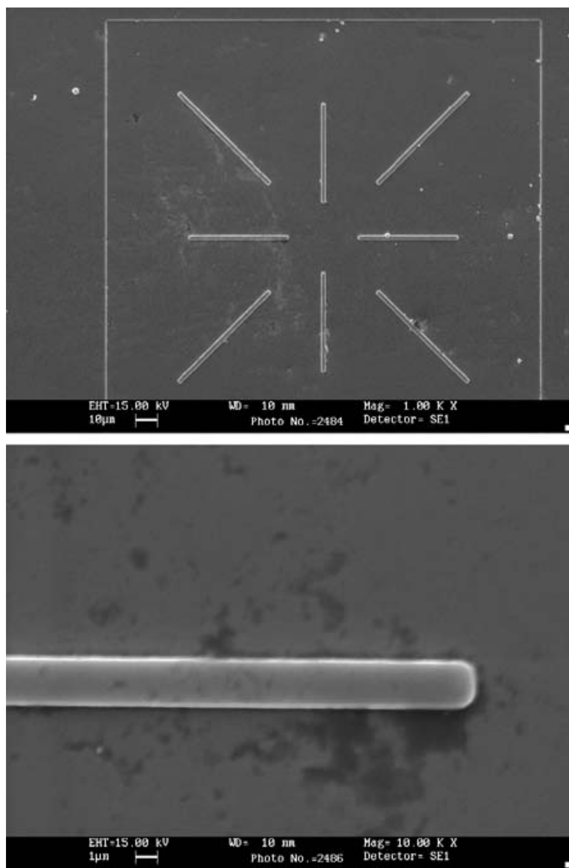

Fig. 5 Figure shows 1.2-μm-thick trenches perfectly filled with copper deposit. The *lower photo* shows an enlargement of one part of the plated detail. Metallic copper does not appear on blocked surface even after complete filling of the surface feature

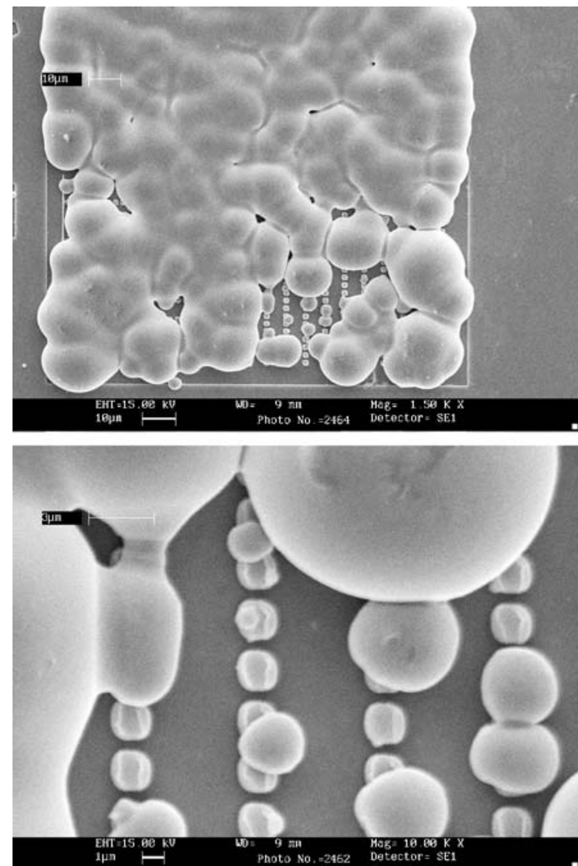

Fig. 6 Overdeposition. Thicker patterns extending over the surface structure are obtained for longer-time deposition. Prolongation of the deposition time in the case of copper deposition onto the surface with small, densely packed features can lead to consolidation of individual copper elements. Process of growing a solid layer of Cu over small individual pits (*upper part*). Hundreds of small features consolidated into one large object due to too long deposition time (*lower part*)

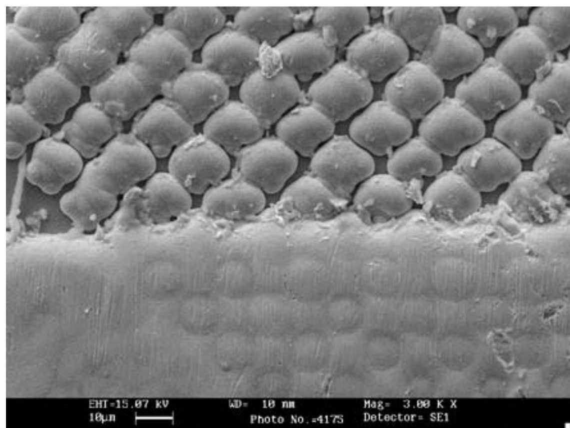

Fig. 7 Border of unblocked and dodecanethiol-blocked surface seen after copper deposition

unblocked surface (lower part of the micrograph), while in the upper part, only the features are filled with Cu.

Conclusions

Localized electrochemical deposition has been extensively investigated in recent years that has resulted in new approaches to surface engineering. The method of surface treatment presented in this paper may simplify the manufacturing process for the electrical connectors used for the power input and the signal management in microelectronic devices. We have employed the practical insolubility of dodecanethiol in water to protect the inside of the trenches against adsorption of dodecanethiol, while the main, flat surface could be blocked by thiols and remained free of copper electrodeposits.

This work has shown that the application of alkanethiols for selectively masking a silicon wafer before copper plating can prevent copper deposition outside the trenches and vias. However, taking into account the very small size of surface features, it is not possible to prevent, for sure, short-circuiting in the copper microstructure. In addition, silicon wafers are copper-seeded (tens-of-angstrom-thick Cu seed layer); thus, the CMP procedure (chemical–mechanical polishing) that follows the electrodeposition step cannot be completely eliminated but may be significantly limited.

The results obtained with the "molecular painting" and described in this paper justify a conclusion that the proposed method may be useful in filling the surface features of size down to the nanometer level.

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